

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listing, of claims in the application:

Listing of claims:

- 1 1. (CURRENTLY AMENDED) A method of fabrication of a capacitor comprising the
2 steps of :
 - 3 a) providing a semiconductor structure having a first region and a
4 capacitor region;
 - 5 b) forming a first conductive layer over said semiconductor structure;
 - 6 c) patterning said first conductive layer to form a plurality of trenches only
7 in said capacitor region and not forming trenches in said first region;
 - 8 d) forming a capacitor dielectric layer over said first conductive layer;
 - 9 e) forming a top plate over said capacitor dielectric layer in the capacitor
10 region;
 - 11 f) patterning said first conductive layer in said first region to form first
12 conductive patterns and a bottom plate;
 - 13 g) forming an interlevel dielectric layer over said first conductive layer.
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2. (ORIGINAL) The method of claim 1 which further includes forming interconnects to
electrically contact said top plate, said bottom plate and said first conductive patterns.
3. (ORIGINAL) The method of claim 1 which further includes:
said first conductive pattern comprise a n-1 level wiring layer;

forming via contacts in said interlevel dielectric layer to contact said top plate, said bottom plate and said first conductive patterns;

forming a second conductive line contacting said via contacts.

4. (ORIGINAL) The method of claim 1 which further includes:

forming via contacts in said interlevel dielectric layer to contact said top plate, said bottom plate and said first conductive patterns;

forming second conductive layer contacting said via contacts; said second conductive layer is a n level metal layer; said first conductive patterns comprise a n-1 level metal layer.

5. (ORIGINAL) The method of claim 1 wherein said first conductive layer is comprised of Al, Ti, Ta, Cu and alloys of Al, Ti, Ta, or Cu; and has a thickness in the range of between 3000 and 10,000 Å.

6. (ORIGINAL) The method of claim 1 wherein said plurality of trenches formed in a pattern of rows and columns.

7. (ORIGINAL) The method of claim 1 wherein said trenches extend down into the conductive layer between 24 % and 84 % of the thickness of said first conductive layer.

8. (CURRENTLY AMENDED) The method of claim 1 wherein step (c) further comprises:

forming a trench resist layer over said first conductive layer; said trench resist layer only has openings that define areas where trenches will be formed in first conductive layer in said capacitor area;

patterning said first conductive layer to form a plurality of trenches only in said capacitor region;

removing said trench resist layer.

9. (ORIGINAL) The method of claim 1 wherein said capacitor dielectric layer has a thickness between 100 and 1000 Å and is comprised of a material selected from the group consisting of silicon oxide, silicon nitride, silicon oxide-nitride, and tantalum oxide.
10. (ORIGINAL) The method of claim 1 wherein said top plate is formed by forming a top plate layer over said capacitor dielectric layer; and masking and patterning said top plate layer.
11. (ORIGINAL) The method of claim 1 wherein step (f) further comprises: forming a bottom metal resist mask over the first conductive layer; the bottom metal resist mask has openings that define the interconnect lines;
- patterning said first conductive layer in said first region to form first conductive patterns and a bottom plate;
- removing said bottom metal resist mask.
12. (ORIGINAL) The method of claim 1 wherein said interlevel dielectric layer is comprised of oxide formed using a high density plasma enhanced chemical vapor silicon oxide deposition combined with plasma enhanced tetraethyl orthosilicate; and interlevel dielectric layer is preferably planarized using a chemical-mechanical polish process.
13. (CURRENTLY AMENDED) A method of fabrication of a capacitor comprising the steps of:
- a) providing a semiconductor structure having a first region and a capacitor region;
 - b) forming a first conductive layer over said semiconductor structure;

- c) forming a trench resist layer over said first conductive layer; said trench resist layer has openings that define areas where trenches will be formed in first conductive layer only in said capacitor area; then
- d) patterning said first conductive layer to form a plurality of trenches in only said capacitor region; then
 - (1) said trenches extend down into the conductive layer between 24 % and 84 % of the thickness of said first conductive layer;
- e) removing said trench resist layer; then
- f) forming a capacitor dielectric layer over said first conductive layer; then
- g) forming a top plate over said capacitor dielectric layer in the capacitor region; said top plate is formed by forming a top plate layer over said capacitor dielectric layer; and masking and patterning said top plate layer; then
- h) patterning said first conductive layer in said first region to form first conductive patterns and a bottom plate; said first conductive patterns comprise a n-l level metal layer;
- i) forming an interlevel dielectric layer over said first conductive layer and said top plate;
- j) forming via contacts in said interlevel dielectric layer to contact said top plate, said bottom plate and said first conductive patterns;
- k) forming second conductive layer contacting said via contacts; said second conductive layer is a n level metal layer.

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14. (ORIGINAL) The method of claim 13 wherein said first conductive layer is comprised of Al, Ti, Ta, Cu and alloys of Al, Ti, Ta, or Cu; and has a thickness in the range of between 3000 and 10,000 Å.
15. (ORIGINAL) The method of claim 13 wherein said plurality of trenches formed in a pattern of rows and columns.
16. (ORIGINAL) The method of claim 13 wherein said top plate is formed by forming a top plate layer over said capacitor dielectric layer; and masking and patterning said top plate layer.
17. (CURRENTLY AMENDED) The method of claim 13 wherein step (h) further comprises:
forming a bottom metal resist mask over the first conductive layer; the bottom metal resist mask has openings only in said first region that define the interconnect lines;
patterning said first conductive layer in said first region to form first conductive patterns and a bottom plate;
removing said bottom metal resist mask.